KAF- 16801LE

4096 (H) x 4096 (V) Pixel

Enhanced Response
Full-Frame CCD Image Sensor
With Anti-Blooming Protection

Performance Specification

Eastman Kodak Company

Image Sensor Solutions

Rochester, New York 14650-2010

Revision 0

August 22, 2000

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

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Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

1.1 Features

- **16M Pixel Area CCD**
- **4096H x 4096V (9 μm) Pixels**
- **36.88 mm H x 36.88 mm V Photosensitive Area**
- **2-Phase Shift Register Clocking**
- **70 % Fill Factor**
- **High Output Sensitivity (12 μV/e-)**
- **Low Dark Current (<10pA/cm^2 @ 25^{o}C)**

1.2 Description

The KAF-16801LE is a high performance monochrome area CCD (charge-coupled device) image sensor with 4096H x 4096V photo active pixels designed for a wide range of image sensing applications in the 0.4nm to 1.0nm wavelength band. Typical applications include military, scientific, and industrial imaging. A 72dB dynamic range is possible operating at room temperature.

The sensor is built with a true two-phase CCD technology employing a transparent gate. This technology simplifies the support circuits that drive the sensor and reduces the dark current without compromising charge capacity. The transparent gate results in spectral response increased ten times at 400nm, compared to a front side illuminated standard poly silicon gate technology. The sensitivity is increased 50% over the rest of the visible wavelengths.

Total chip size is 38.60 mm x 37.76 mm and is housed in a 34-pin, 2.010" wide DIL ceramic package with 0.1" pin spacing.

The sensor consists of 4127 parallel (vertical) CCD shift registers each 4128 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The elements of these registers are arranged into a 4096 x 4096 photosensitive array surrounded by a light shielded dark reference of 29 columns and 30 rows. There is a buffer region of one photosensitive pixel surrounding the photosensitive region (one column at the beginning of a line, one column at the end of a line, one row at the beginning of a frame, and one row at the end of a frame). The parallel (vertical) CCD registers transfer the image one line at a time into a single 4145 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a three-stage source follower that converts the photo-generated charge to a voltage for each pixel.

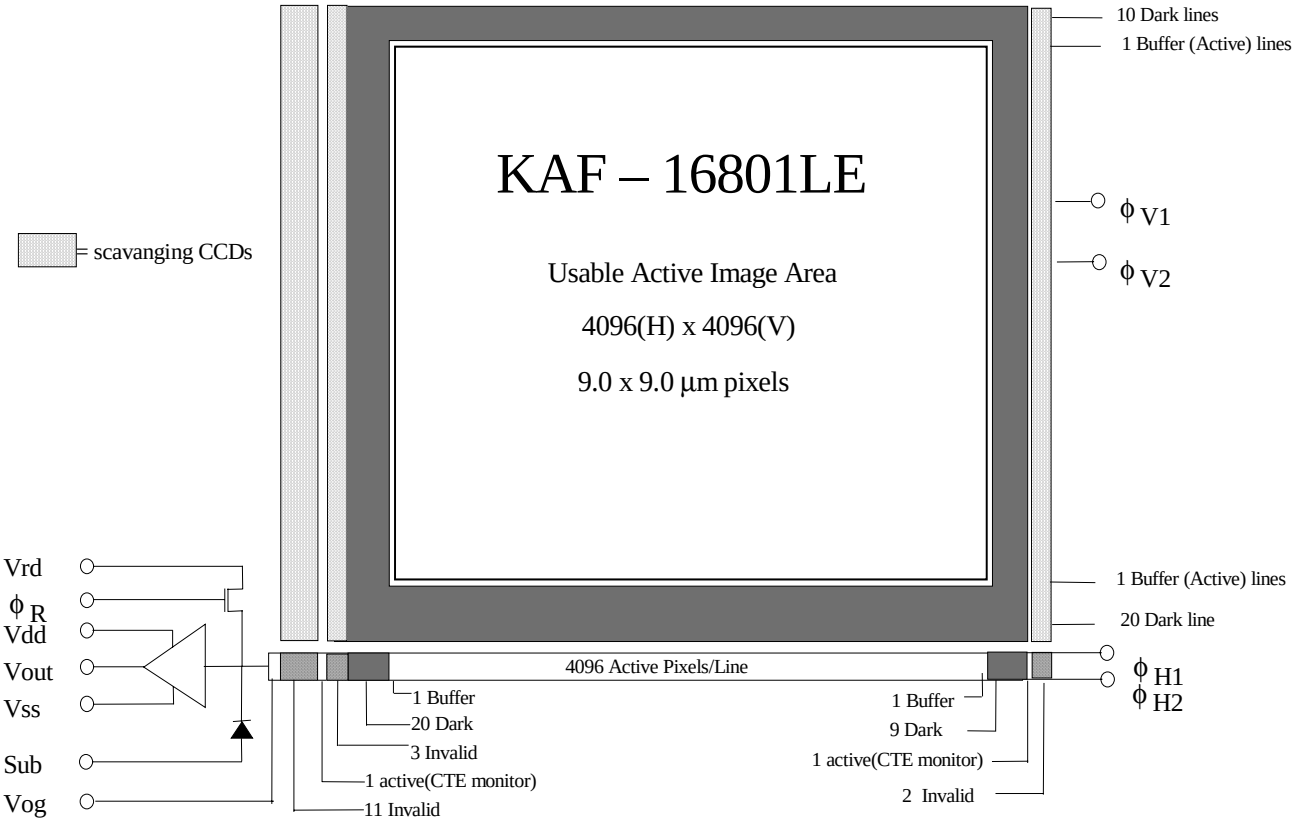

Figure 1 - Functional Block Diagram

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1.3 Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will be removed by the anti-blooming drain that is integrated into each pixel. During the integration period, the ϕV1 and ϕV2 register clocks are held at a constant (low) level.
See Figure 5. - Timing Diagrams.

1.4 Charge Transport

Referring again to Figure 5 - Timing Diagrams, the integrated charge from each photogate is transported to the output using a two step process. Each line (row) of charge is first transported from the vertical CCDs to the horizontal CCD register using the ϕV1 and ϕV2 register clocks. The horizontal CCD is presented a new line on the falling edge of ϕV1 while ϕH2 is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the ϕH1 and ϕH2 pins in a complementary fashion. On each falling edge of ϕH1 a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

1.5 Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on FD. Once the signal has been sampled by the system electronics, the reset gate (ϕR) is clocked to remove the signal and FD is reset to the potential applied by Vrd. More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device - see Figure 4.

1.6 Dark Reference Pixels

Surrounding the peripheral of the device is a border of light shielded pixels. This includes 20 leading and 10 trailing pixels on every line excluding the inactive and photosensitive buffer pixels. There are also 20 full dark lines at the start of every frame and 10 full dark lines at the end of each frame. Under normal circumstances, these dark reference pixels do not respond to light. However, the pixels in close proximity to an active pixel, or the outer bounds of the can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

1.7 Transfer Efficiency Test Pixels and Dummy Pixels

At the beginning of each line and at the end of each line are extra horizontal CCD pixels. These are a combination of pixels that are not associated with any vertical CCD register and two that are associated with extra photo active vertical CCDs. The two extra photo active vertical CCDs are provided to give an accurate photo generated signal that can be used to monitor the charge transfer efficiency in the serial (horizontal) register.

They are arranged as follows beginning with the first pixel in each line

11 dark, inactive pixels
1 photo active test pixel
3 inactive pixels
20 dark reference pixels
1 active buffer pixel
4096 photoactive pixels
1 active buffer pixel
9 dark reference pixels
1 photo active test pixel
2 inactive pixels

2.1 Package Drawing

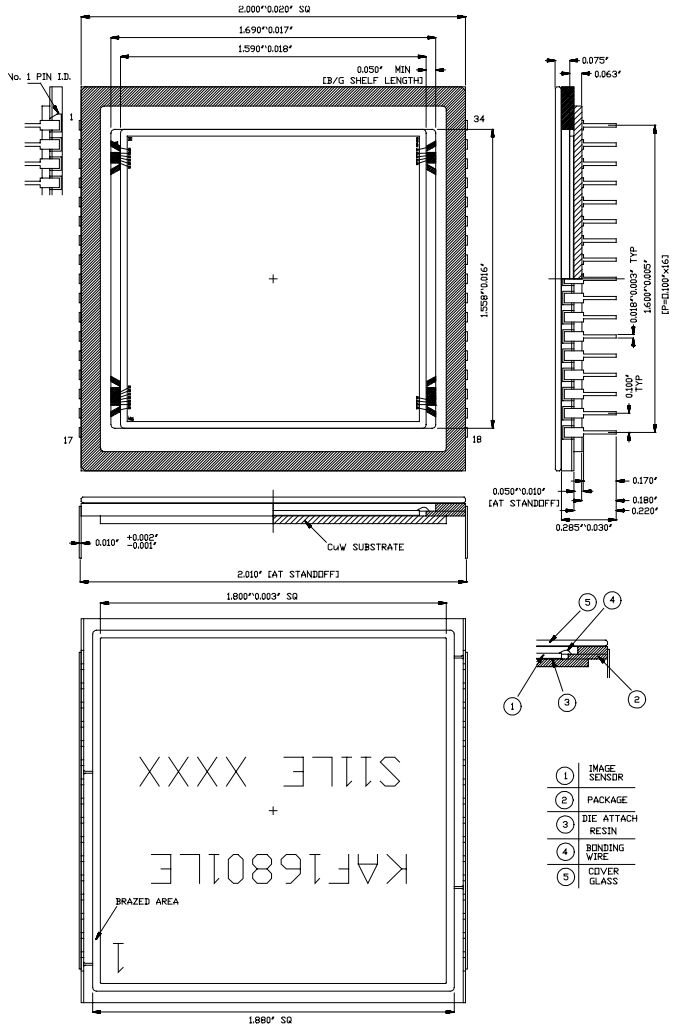

Figure 2 - Package Drawing

2.2 Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1, 11, 18, 30	Vsub	Substrate (Ground)	14	Vout	Video Output
2, 3, 33, 34	ϕ_{V2}	Vertical CCD Clock - Phase 2	15	Vss	Amplifier Supply Return
4, 5, 31, 32	ϕ_{V1}	Vertical CCD Clock - Phase 1	16	Vrd	Reset Drain
6	Vguard	Guard Ring / Anti blooming drain	17	ϕR	Reset Clock
7, 8, 9, 10, 22, 23, 24, 25, 26, 27, 28, 29	N/C	No connection (open pin)	19	ϕ_{H1}	Horizontal CCD Clock - Phase 1
12	Vog	Output Gate	20	ϕ_{H2}	Horizontal CCD Clock - Phase 2
13	Vdd	Amplifier Supply	21	N/C	No Connect

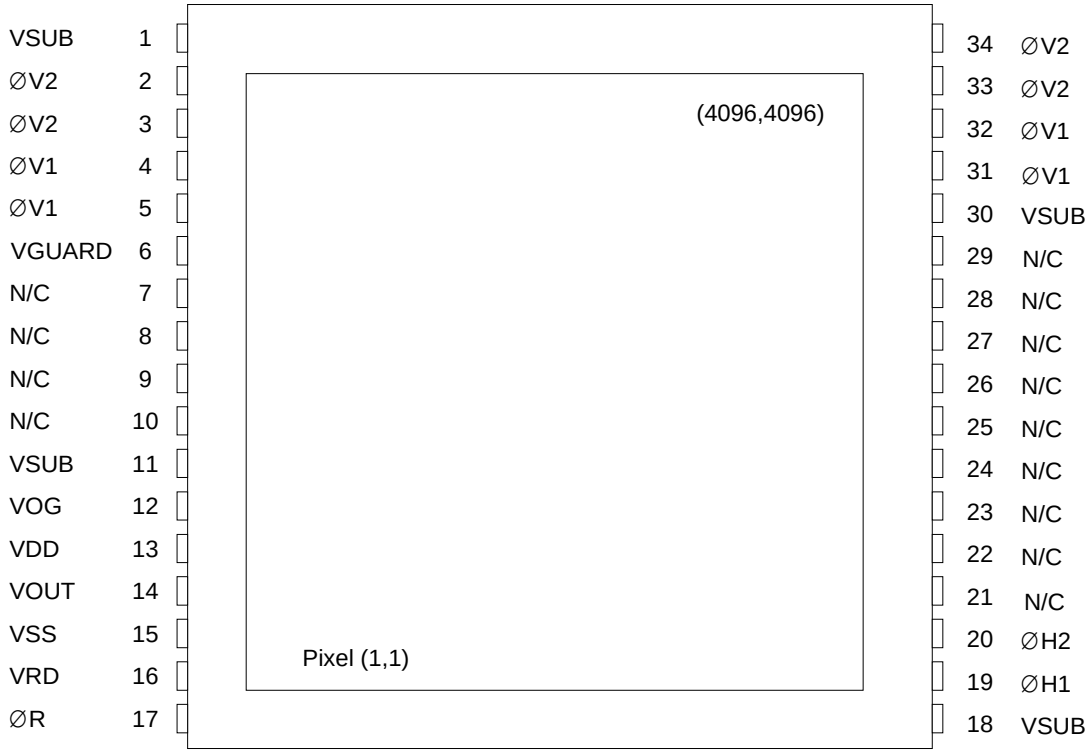

Figure 3 - Package Pin Designations

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3.1 Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Units	Notes
Diode Pin Voltages	Vdiode	0	20	V	1, 2
Gate Pin Voltages - Type 1	Vgate1	-16	16	V	1, 3
Gate Pin Voltages - Type 2	Vgate2	0	16	V	1, 4
Inter-Gate Voltages	Vg-g		16	V	5
Output Bias Current	Iout		-10	mA	6
Output Load Capacitance	Cload		15	pF	6
Storage Temperature	T	-50	70	^{o}C	
Humidity	RH	5	90	%	7

Notes:
1. Referenced to pin Vsub.
2. Includes pins: Vrd, Vdd, Vss, Vout, Vguard.
3. Includes pins: ϕV1, ϕV2, ϕH1, ϕH2.
4. Includes pins: ϕR, Vog
5. Voltage difference between overlapping gates. Includes: ϕV1 to ϕV2, ϕH1 to ϕH2, ϕV1 to ϕH2, ϕH1 to Vog.
6. Avoid shorting output pins to ground or any low impedance source during operation.
7. T=25°C. Excessive humidity will degrade MTTF.

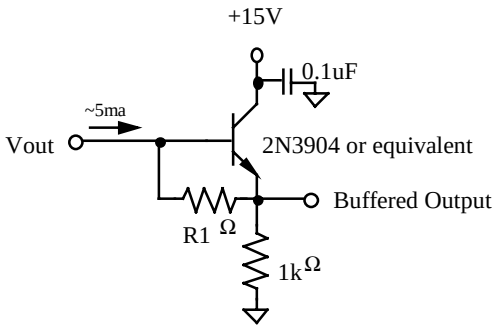
CAUTION: This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance with strict ESD procedures for Class 1 devices.

3.2 DC Operating Conditions

Description	Symbol	Min	Nom	Max	Unit	Max DC Current (mA)	Notes
Reset Drain	Vrd	11	12	12.25	V	0.01	
Output Amplifier Return	Vss	1.5	2.0	2.5	V	0.45	
Output Amplifier Supply	Vdd	14.5	15	15.5	V	Iout	
Substrate	Vsub	0	0	0	V	0.01	
Output Gate	Vog	4.25	4.5	5.0	V	0.01	
Guard Ring	Vguard	9.0	10.0	12.0	V	0.01	
Video Output Current	Iout	-3.5	-5	-10	mA	-	1

Notes:

1. An output load sink must be applied to Vout to activate output amplifier - see Figure below.



The value of R1 depends on the desired output current according the following formula: R1 = 0.7 / Iout
The optimal output current depends on the capacitance that needs to be driven by the amplifier and the bandwidth required. 5 mA is recommended for capacitance of 12 pF and pixel rates up to 20 MHz.

Figure 4 – Typical Output Structure Load Diagram

(For operation of up to 10 MHz)

3.3 AC Operating Condition

Description	Symbol	Level	Min.	Nom.	Max.	Units	Effective Capacitance	Notes
Vertical CCD Clock - Phase 1	ϕV1	Low High	-9.0 ϕV1 low + 10.5	-8.5 2.0	-8.3 ϕV1 low + 10.5	V V	250nF (all ϕV1 pins)	
Vertical CCD Clock - Phase 2	ϕV2	Low High	-9.0 ϕV2 low + 10.5	-8.5 2.0	-8.3 ϕV2 low + 10.5	V V	250nF (all ϕV2 pins)	
Horizontal CCD Clock - Phase 1	ϕH1	Low High	-2.5 ϕH1 low + 10.5	-2.5 8.0	-1.8 ϕH1 low + 10.5	V V	500pF	
Horizontal CCD Clock - Phase 2	ϕH2	Low High	-2.5 ϕH2 low + 10.5	-2.5 8.0	-1.8 ϕH2 low + 10.5	V V	300pF	
Reset Clock	ϕR	Low High	3.0 9.5	5.0 10.0	5.5 10.5	V V	10pF	

Notes:
1. All pins draw less than 10uA DC current.
2. Capacitance includes gate to VSUB and gate to gate (V1-V2, H1-H2).

3.4 AC Timing Conditions

Description	Symbol	Min.	Nom.	Max.	Units	Notes
ϕH1, ϕH2 Clock Frequency	f_H		8	15	MHz	1, 2, 3
ϕV1, ϕV2 Clock Frequency	f_V		25	25	kHz	1, 2, 3
Pixel Period (1 Count)	t_e	67	125		ns	
ϕH1, ϕH2 Setup Time	$t_{\phi HS}$	0.5	1		us	
ϕV1, ϕV2 Clock Pulse Width	$t_{\phi V}$	40	40		us	
ϕV1, ϕV2 Clock Pulse Overlap	$t_{\phi Vovrlp}$	20	20		us	
Reset Clock Pulse Width	$t_{\phi R}$	10	20		ns	4
Readout Time	$t_{readout}$	1398	2390		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	338.7	580		µs	7

Notes:
1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Cross-over of register clocks should be between 40-60% of amplitude.
4. ϕR should be clocked continuously.
5. $t_{readout} = (4128 * t_{line})$
6. Integration time is user specified. Longer integration times will degrade noise performance.
7. $t_{line} = (2* t_{\phi V}) - t_{\phi Vovrlp} + t_{\phi HS} + (4145 * t_e) + t_e$

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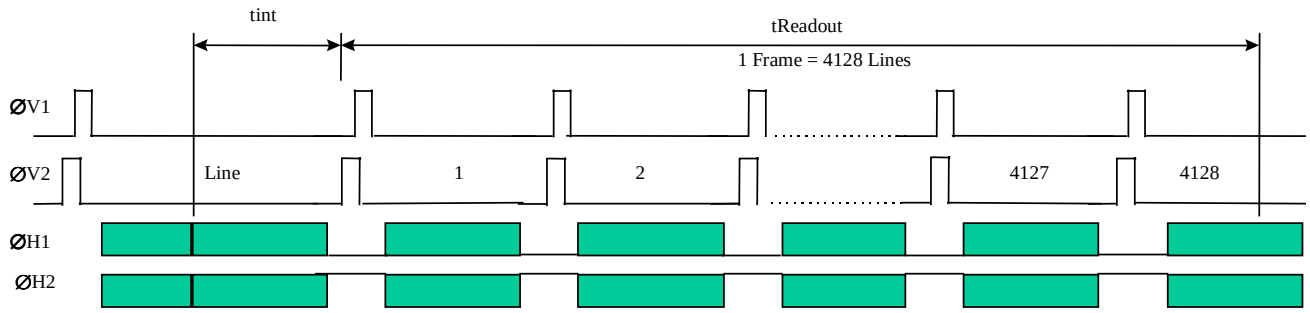
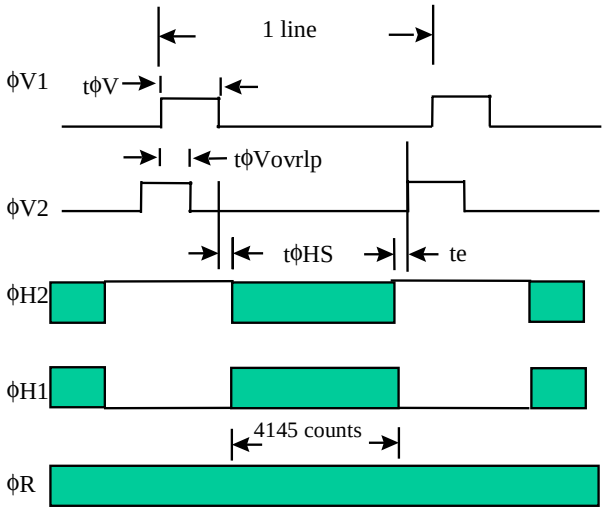
3.5 Clock Timing

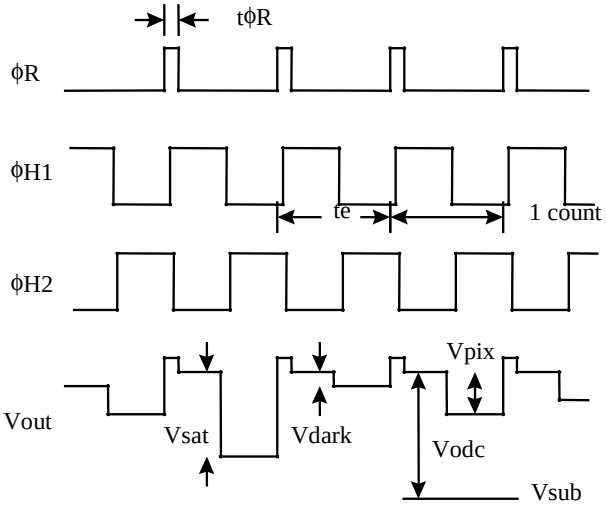
Frame Timing



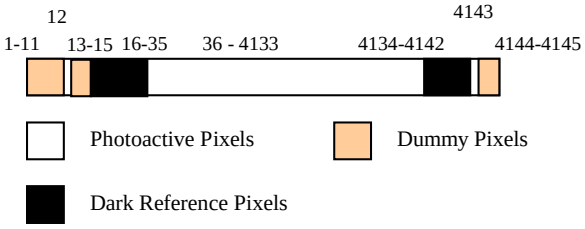
Line Timing Detail



Pixel Timing Detail



Line Content



Vsat	Saturated pixel video output signal
Vdark	Video output signal in no light situation, not zero due to Jdark
Vpix	Pixel video output signal level, more electrons =more negative'
Vodc	Video level offset with respect to vsub
Vsub	Analog Ground

* See Image Aquisition section (page 4)

Figure 5 Timing Diagram

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4.1 Performance Specification

All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Saturation Signal Vertical CCD capacity Horizontal CCD capacity Output Node capacity	Nsat	 45000 170,000 180,000	 55000 180000 220000	 250000	electrons / pixel	 1
Spectral Sensitivity See section 4.2.1						
Photoresponse Non-Linearity	PRNL		1	2	%	2
Photoresponse Non-Uniformity	PRNU		1	3	%	3,11
Dark Signal	Jdark		15 3.5	35 7	electrons / pixel / sec pA/cm^2	4
Dark Signal Doubling Temperature		5	6.3	7.5	^{o}C	
Dark Signal Non-Uniformity	DSNU		15	35	electrons / pixel / sec	5,11
Dynamic Range	DR	67	71		dB	6
Charge Transfer Efficiency	CTE	0.99997	0.99999			
Output Amplifier DC Offset	Vodc	Vrd-3	Vrd – 2.5	Vrd-2	V	7
Output Amplifier Bandwidth	f_{-3dB}		140		Mhz	8
Output Amplifier Sensitivity	Vout/Ne$^-$	12.5	13	14	uV/e-	
Output Amplifier output Impedance	Zout		130		Ohms	
Noise Floor	ne$^-$		15	20	electrons	9
Antiblooming Protection	Vab	128			Saturation exposure	10

Notes:

1. For pixel binning applications, electron capacity up to 270000 can be achieved with modified CCD inputs. Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
2. Worst case deviation from straight line fit, between 1% and 90% of Vsat.
3. One Sigma deviation of a 128x128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25 ^{o}C..
5. Average dark signal of any of 32 x 32 blocks within the sensor. (each block is 128 x 128 pixels)
6. 20log (Nsat / ne~) at nominal operating frequency and 25^{o}C.
7. Video level offset with respect to ground
8. Assumes 10pF off-chip load.
9. Output amplifier noise at 25^{o}C,operating at pixel frequency up to 2MHz, bandwidth =20MHz , tint = 0, and no dark current shot noise.
10. Number of times above the Vsat illumination level required to cause 50% distortion in a test pattern consisting of a bright circular region approximately 1/10 the size of the image sensor. In most systems a 128x optical overload will cause flare from reflections that mask the performance of the image sensor. Assumes an integration time >15msec. For integration times <15msec the photo current in the overexposed region may be high enough to cause the anti blooming protection to be reduced below the minimum value specified.
11. Specification excludes region [1,1,400,400]. See section 4.2.2.

4.2 Spectral Response

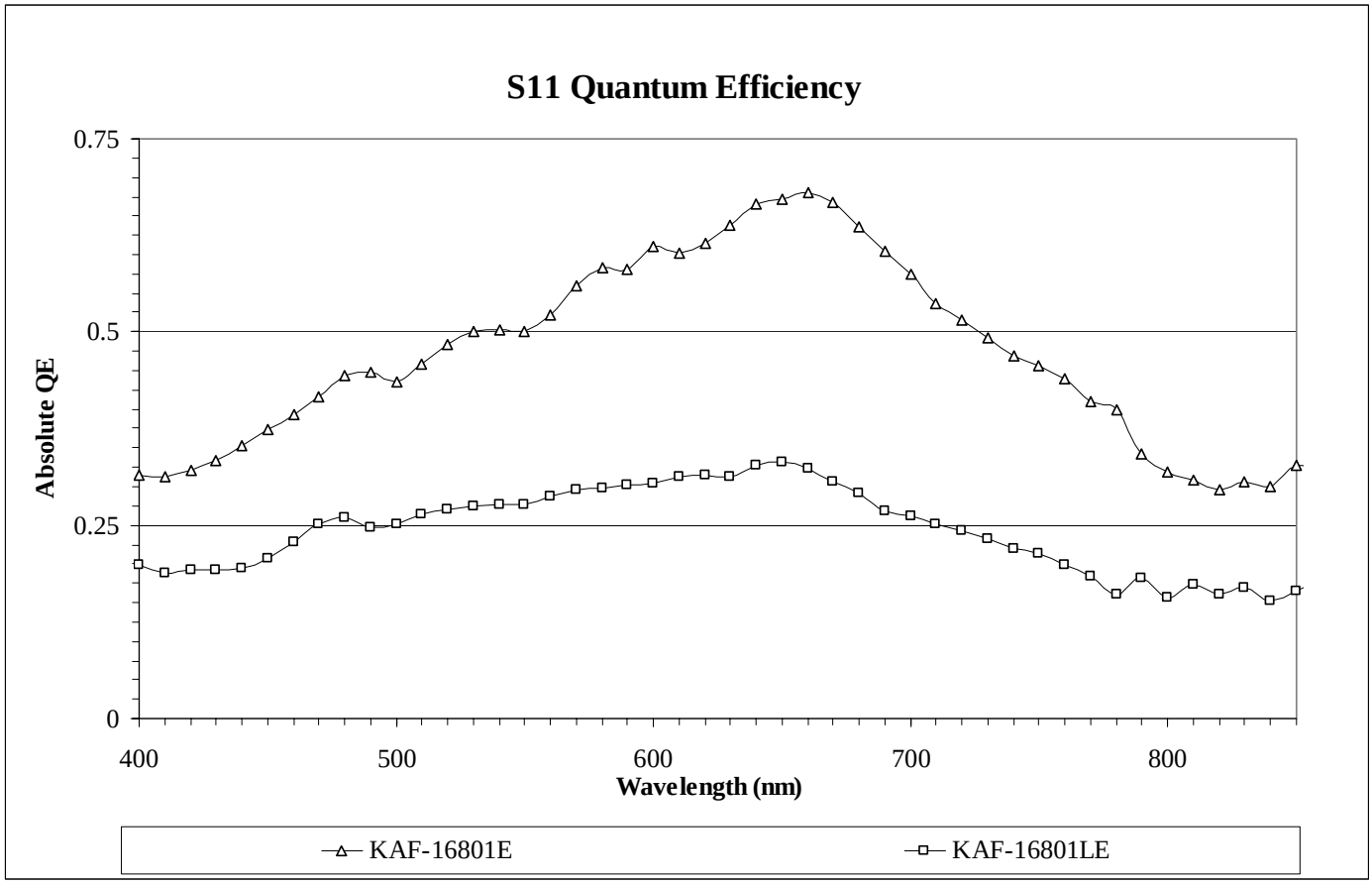
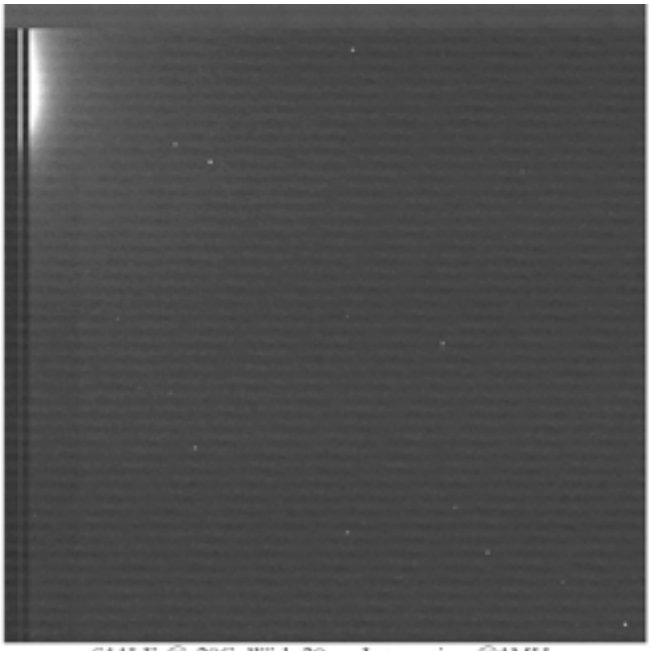


Figure 6 - Spectral response

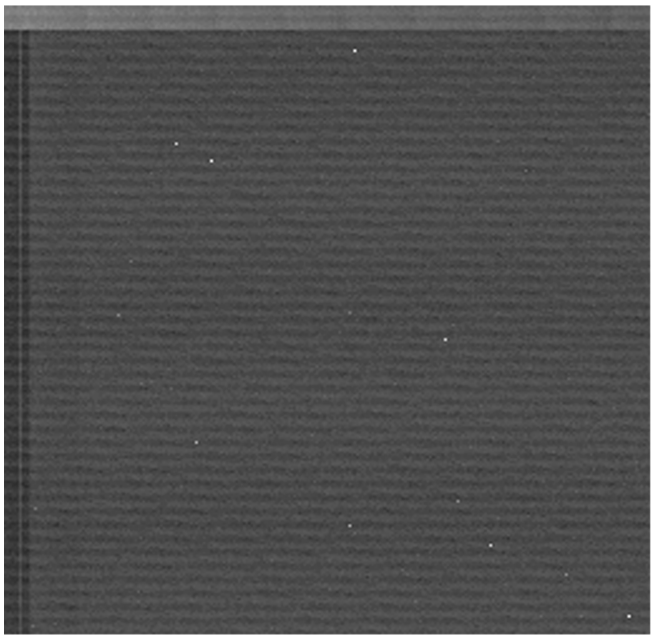
4.2.1 Dark current non-uniformity

The photoresponse non-uniformity specification and the dark signal non-uniformity specification of the sensor both exclude the region that is [1,1,400,400]. The reason for this exclusion is that when the sensor is running with VDD always on, and the integration times are greater than 100msec, a non-uniformity will become evident surrounding the first pixel. This non-uniformity is a result of the output amplifier emitting light into the photoactive area, see Figure 7. The elevated dark signal in this region typically ranges from 30 electrons/pixel/sec to 100 electrons/pixel/sec depending on the part and is independent of temperature. If VDD is switched to 0volts at least 10 µsec after the last pixel is read out and switched back to full value 10 µsec before the first pixel of the next frame, the effect of the amplifier glow will be eliminated, see Figure 8.



S11LE @-20C With 20sec Integration @1MHz
VDD Always On (+15)

Figure 7 Amplifier glow



S11LE @-20C With 20sec Integration @1MHz
VDD Off During Integration

Figure 8 Amplifier glow suppressed by switching VDD to 0 volts during integration.

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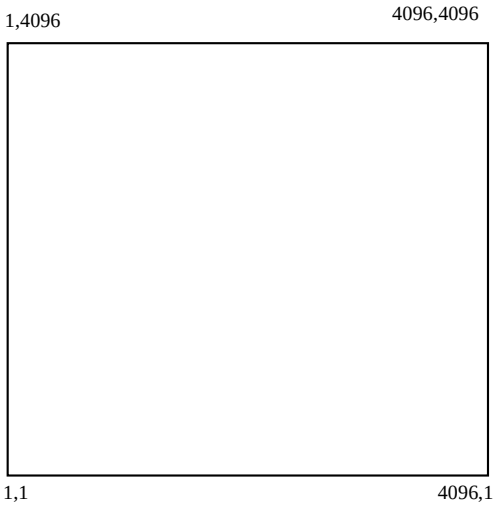
4.3 Cosmetic Classification

Defect tests performed at T=25°C

Grade	Point Defects	Cluster Defects	Maximum Cluster Size	Column Defects	Maximum Column Width
C1	≤60	≤8	8	4	1
C2	≤120	≤16	8	10	1
C3	≤240	≤32	15	20	2



Point Defect	Dark: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation, OR Bright: A Pixel with dark current > 7,000 e/pixel/sec at 25C.
Cluster Defect	A grouping of not more than 5 adjacent point defects
Column Defect	A grouping of >5 contiguous point defects along a single column, OR A column containing a pixel with dark current > 20,000e/pixel/sec, OR A column that does not meet the CTE specification for all exposures less than the specified Max sat. signal level and greater than 2 Ke, OR A pixel which loses more than 250 e under 2Ke illumination.
Neighboring pixels	The surrounding 128 x 128 pixels or ±64 columns/rows.
Defect Separation	Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).
Defect Region Exclusion	Defect region excludes the outer two (2) rows and columns at each side/end of the sensor.

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5.1 Quality Assurance and Reliability

5.1.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.

5.1.2 Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale.

5.1.3 Cleanliness: Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.

5.1.4 ESD Precautions: Devices are shipped in a static-safe container and should only be handled at static-safe work stations.

5.1.5 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request.

5.1.6 Test Data Retention: Devices have an identifying number of traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

5.2 Ordering Information

See Appendix 1 for available part numbers

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (716) 722-4385
Fax: (716) 477-4947
Web: www.kodak.com/go/ccd
E-mail: ccd@kodak.com

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WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

Appendix 1

Part Number Availability

Note: This appendix may be updated independently of the performance specification. Contact Eastman Kodak for the latest revision

Device Name	Available Part Numbers	Features
KAF-16801LE	2H4778	Monochrome LOD Enhanced, Clear Taped Cover Glass, Engineering Grade
KAF-16801LE	2H4779	Monochrome LOD Enhanced, Clear Taped Cover Glass, Mechanical Grade
KAF-16801LE	2H4784	Monochrome LOD Enhanced, Clear Sealed Cover Glass, Engineering Grade
KAF-16801LE	2H4785	Monochrome LOD Enhanced, Clear Sealed Cover Glass, Mechanical Grade

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